AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Previously presented)* A backplane comprising:

an array of electrical or electronic elements, each of said electrical or electronic elements comprising at least a first electronic element layer and a second electronic element layer; and

and at least one separate spacer which rises higher over the backplane than said array said at least one spacer comprises at least a first spacer layer and a second spacer layer wherein said first spacer layer is formed from substantially the same material as said first electronic element layer and said second spacer layer is formed from substantially the same material as said second electronic element layer and wherein said first and second spacer layers are in the same order in the spacer as first and second electronic element layers appear in said electrical or electronic elements.

2. *(Original)* A backplane according to claim 1 wherein the backplane is a semiconductor backplane.

3. *(Previously presented)* A backplane according to claim 1 wherein said at least one spacer includes at least one additional space layer, said at least one additional spacer layer and said first and second spacer layers forming a series of more than two layers.

4. *Canceled.*

5. *(Previously presented)* A backplane according to claim 1 wherein all the layers in the spacer correspond in material and order to all the layers in said at least one electrical or electronic element.

6. *(Previously presented)* A backplane according to claim 1 wherein the spacer is electrically insulating between a top and bottom of said spacer.

7. *(Previously Presented)* A backplane according to claim 1 wherein there is a plurality of said spacers distributed over the backplane.

8. *(Original)* A backplane according to claim 7 wherein at least some of the spacers are regularly distributed over the array.

9. *(Previously Presented)* A backplane according to claim 7 wherein the array provides a plurality of addressable locations, and each location has at least one said spacer associated therewith.

10. *(Original)* A backplane according to claim 9 wherein each location has only one said spacer associated therewith.

11. *(Previously Presented)* A backplane according to claim 7 wherein at least one said spacer is in the form of a column having a generally square cross-section.

12. *(Previously Presented)* A backplane according to claim 7 wherein at least one said spacer is in the form of a ridge having an elongate cross-section.

13. *(Previously Presented)* A backplane according to claim 1 wherein said array is covered by an insulating layer which also extends over the said spacer or said plurality of spacers.

14. *(Original)* A backplane according to claim 13 wherein said insulating layer has a generally constant thickness.

15. *(Original)* A backplane according to claim 13 wherein the upper surface of said insulating layer is substantially flat.

16. *(Previously Presented)* A backplane according to claim 13 wherein an electrode is deposited on said insulating layer and is coupled to a said element of said array.

17. *(Original)* A backplane according to claim 16 wherein said electrode is reflective.

18. *(Original)* A backplane according to claim 17 wherein the reflectivity of the electrode is greater than the reflectivity of conductive layers occurring in the electrical or electronic element and/or spacers of the array.

19. *(Previously Presented)* A backplane according to claim 1 wherein the top surface thereof is treated in a manner to induce liquid crystal alignment.

20. *(Previously Presented)* A backplane according to claim 1 wherein the backplane is an active backplane in which the array comprises active electronic elements.

21. *(Previously Presented)* A backplane according to claim 1 wherein at least some of the spacers are located externally of the array.

22. *(Previously Presented)* A backplane according to claim 1 wherein the array is connected to other circuitry formed on the backplane but spaced from the array by a lane.

23. *(Previously presented)* A backplane according to claim 22 wherein said externally located spacers are located in said lane.

24. *(Previously Presented)* A backplane according to claim 22 wherein the said lane is of sufficient width to permit the presence of an adhesive sealing strip without substantial contact with the array and said other circuitry.

25. *(Previously Presented)* A backplane according to claim 22 wherein the width of the lane is least 500 microns.

26. *(Original)* A backplane according to claim 25 wherein the width of the lane is least 1500 microns.

27. *(Previously Presented)* A backplane according to claim 22 wherein the said circuitry connected to the array comprises logic for addressing elements of the array.

28. *(Previously Presented)* A method of producing a backplane as defined in claim 1, wherein processes used for making parts of at least one said element are also used simultaneously to form parts of said spacers.

29. *(Currently Amended)* A method of producing a backplane having at least one region containing an array of electrical or electronic elements and at least one separate spacer which rises higher over the backplane than said elements, said at least one spacer being laterally spaced from said elements, wherein the processes used for making parts of at least one said element are also used simultaneously to form parts of said at least one spacer~~spacers on the backplane laterally spaced from said elements~~.

30. *(Original)* A method according to claim 29 wherein said backplane is a semiconductor backplane.

31. *(Previously Presented)* A method of producing a backplane according to claim 29 wherein the spacers comprise at least two layers of substantially the same material and occurring in the same order as is found in at least one said electrical or electronic element.

32. *(Previously Presented)* A cell comprising a backplane as defined in claim 1 and an opposed electrode sealed thereto in spaced relation.

33. *(Previously Presented)* A cell according to claim 32 wherein liquid crystal material is located between the electrode and the backplane.

34. *(Original)* A cell according to claim 33 wherein the liquid crystal material has a smectic phase.